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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,626	06/20/2003	Archer Lawrence	KIN03003	7189

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HAMILTON & TERRILE, LLP
P.O. BOX 203518
AUSTIN, TX 78720

EXAMINER	
PRETLOW, DEMETRIUS R	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 11/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,626	LAWRENCE ET AL.	
	Examiner	Art Unit	
	Demetrius R. Pretlow	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4,5,9 and 15-17* is/are allowed.

6)☒ Claim(s) *6,10,12 and 14* is/are rejected.

7)☒ Claim(s) *7,8,13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6,10,12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over WU 5,831,992. in view of Arkin (US 6,380,730). In reference to claim 6, a vector generator (12) operable to generate test data and apply the test data to the electronic device to determine the response of the electronic device; Note Wu column 3, lines 53-58. Wu teach a capture interface operable to capture the test data communicated to the electronic device by the tester;(performed by the self test of the integrated circuit) Note Wu column 4, lines 6,7 and 12. Wu teach a compression engine (14) in communication with the capture interface and operable to compress the test data; Note column 4, lines 12-14 and lines 48-54. Wu teach a memory in communication with the compression engine and operable to save the compressed test data. Note Wu column 4, lines 26-28.

Wu does not teach wherein the electronic device comprises a memory device operable to store data fields according to address and control information and the vector generator generates memory vectors for storage on the memory device.

Arkin et al. (US 6,380,730) teach wherein the electronic device comprises a memory device operable to store data fields according to address and control

Arkin et al. (US 6,380,730) teach the electronic device comprises a memory device and generating test data further comprises generating vectors of memory test data for storage on the memory device, (Note column 8, 4, lines 19-20) the memory test data having data field, address and control information. (Note column 4, lines 63-67 and column 5, lines 1-12)

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Wu to include the teaching of Arkin et al. because it would help determine whether a memory storage location within the memory is defective at that address. Note column 5, lines 14-15.

In reference to claim 12, Wu does not teach reading test data stored on the memory device; comparing the read test data with the test data written to the memory device; and detecting an error if the read test data differs from the written test data.

Arkin et al. teach reading test data stored on the memory device; comparing the read test data with the test data written to the memory device; and detecting an error if the read test data differs from the written test data. Note column 4, lines 60-63.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Wu to include the teaching of Arkin et al. because it would help determine whether a memory storage location within the memory is defective at that address. Note column 5, lines 14-15.

In reference to claim 14, Wu does not teach detecting repeat patterns; and representing the repeat patterns with the repeated value and a count of the number of repeat of the repeat value.

information (Note column 4, lines 63-67 and column 5, lines 1-12) and the vector generator generates memory vectors for storage on the memory device. Note column 8, 4, lines 19-20.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Wu to include the teaching of Arkin et al. because it would help determine whether a memory storage location within the memory is defective at that address. Note column 5, lines 14-15.

In reference to claim 10, Wu teach generating test data for application to the electronic device; Note Wu column 3, lines 53-58. Wu teach communicating the test data to the electronic device through an interface; (performed by the self test of the integrated circuit) Note Wu column 4, lines 6,7 and 12. Wu teach capturing the test data communicated to the electronic device; (performed by the self test of the integrated circuit) Note Wu column 4, lines 6,7 and 12. Wu teach compressing the captured test data; Note column 4, lines 12-14 and lines 48-54. Wu teach storing the compressed test data; Note Wu column 4, lines 26-28. Wu teach detecting the error response by the electronic device to the test data. Note column 6, lines 11-12. Wu teach analyzing the compressed test data to identify the source of the error response. Note Note column 7, lines 34-36.

Wu does not teach where the electronic device comprises a memory device and generating test data further comprises generating vectors of memory test data for storage on the memory device, the memory test data having data field, address and control information.

Arkin et al. teach detecting repeat patterns; and representing the repeat patterns with the repeated value and a count of the number of repeat of the repeat value. Note claim 7, lines 6-15.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Wu to include the teaching of Arkin et al. because it would help determine whether a memory storage location within the memory is defective at that address. Note column 5, lines 14-15.

Claims 7,8,13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

Claims 1,4,5,9,15, and 16 are allowed.

The primary reason for the allowance of claims 1,4 and 5 is the inclusion of the limitations of an analyzer interfaced with the decompression engine and operable to analyze the de compressed test data to determine the test data source of an electronic device error response, the analyzer-further operable to generate a test program that reduces the empty cycles of the test data. It is these limitations found in each of the claims, as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for the allowance of claim 9 is the inclusion of the limitations of an is the inclusion of the limitations of an wherein the memory further comprises plural memory motherboards; a memory parser associated with each memory motherboard; plural memory controllers associated with each memory parser; and plural memory storage devices associated with each memory controller; wherein the memory parser coordinates with its associated memory controllers to store test data on plural memory storage devices in sequence so that the memory storage devices operate on a lower clock speed than the test data generation clock speed. It is these limitations found in each of the claims, as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for the allowance of claim 15 is the inclusion of the method steps of wherein storing the compressed test data further comprises coordinating storage of the test data in plural storage devices so that the storage devices operate at a slower clock speed than the clock speed associated with the generation of the test data. It is this step found in each of the claims, as it is **claimed in the combination**, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for the allowance of claims 16-17 is the inclusion of the method step of de-compressing the compressed test data to replay the test data applied to the electronic device; and passing the replayed test data through a logic analyzer to determine the applied test data that generated an error response. It is these

steps found in each of the claims, as it is **claimed in the combination**, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

Response to Arguments

Applicant's arguments with respect to claims 6,10,12 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetrius R. Pretlow whose telephone number is (571) 272-2278. The examiner can normally be reached on Mon.-Fri. 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Demetrius R. Pretlow Demetrius Pretlow 11/8/05

MICHAEL NGHIEM
PRIMARY EXAMINER